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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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02/09/2004

Perry Scott Lorenz

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04/18/2011

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EXAMINER

ALMO, KHAREEM E

ART UNIT

PAPER NUMBER

2816

MAIL DATE

DELIVERY MODE

04/18/2011

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/774,799	Applicant(s) LORENZ, PERRY SCOTT	
	Examiner KHAREEM E. ALMO	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☒ Claim(s) 33 and 34 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/28/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura (US 20040174206) in view of La Rosa (US 6897689).

FIG.1

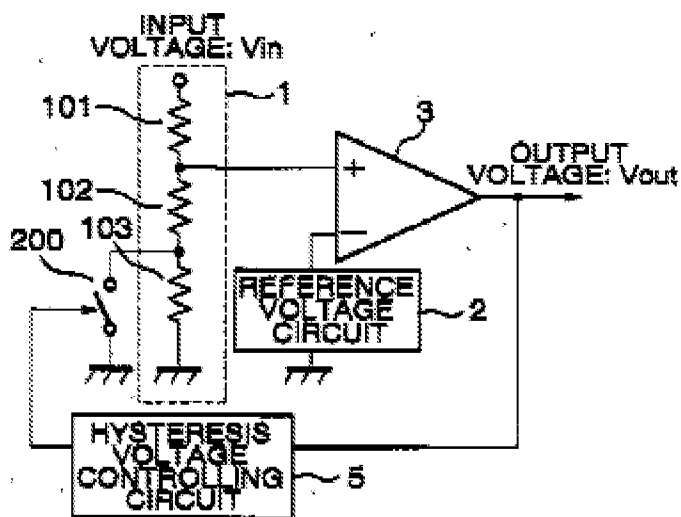
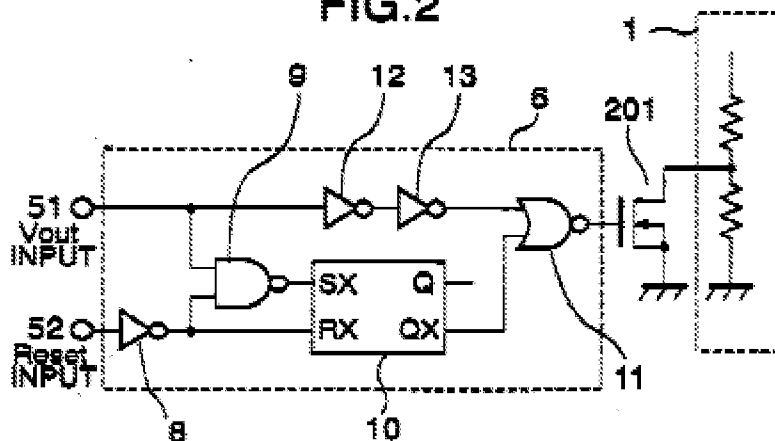


FIG.2



With respect to claim 1, figure 1 and 2 of Matsumura (US 6163183) discloses a circuit for temperature sensing, comprising: a comparator circuit (3 of fig 1) that is arranged to provide a trigger signal by comparing a reference signal (2) to a temperature sensor signal (1); a gate circuit (201 of fig 2 or 200 of fig 1) that is arranged to provide an output signal (V_{out}) by gating a gate input signal (V_{in}) subject to control

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by a gate Control signal (from 5 fig 1 or from 6 fig 2), wherein the gate input signal is based at least in part on the trigger signal (51 fig 2), and wherein the gate control signal is based at least in part on a power-on-reset signal (52 of fig 2); and a hysteresis-and-output-sensor circuit (5 fig 1 or 6 fig 2) that is configured to control the reference signal in response to a sensed signal, wherein the sensed signal is based at least in part on the output signal (Vout), and wherein the hysteresis-and-output sensor circuit is arranged to disable a hysteresis at power up but fails to disclose a power-on-reset generator that is arranged to provide a power-on reset signal.

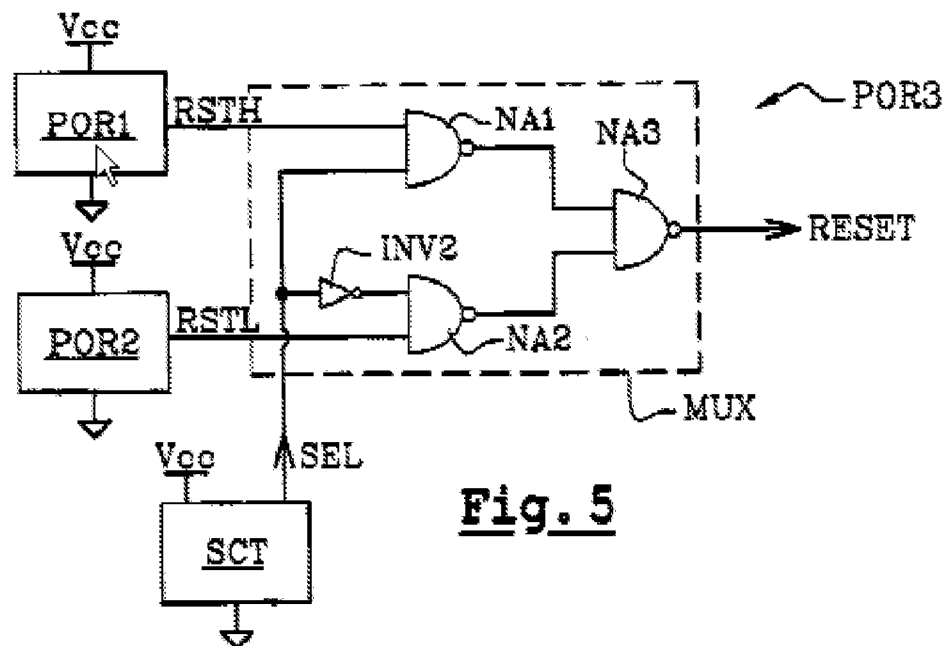
**Fig. 5**

Figure 5 of La Rosa (US 6897689) discloses a POR circuit to generate a reset signal. It would have obvious at the time the invention was made to a person having ordinary skill in the art to use the POR reset circuit of Rosa in the Voltage detecting

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circuit of Matsumura for the purpose of incorporating a POR circuit into an integrated circuit that can receive different supply voltages.

With respect to claim 2, the combination above produces the circuit of Claim 1, wherein the power-on-reset (Fig 5 of La Rosa) signal is the gate control signal.

With respect to claim 3, the combination above discloses the circuit of Claim 1, further comprising: a timer circuit (SCT) that is configured to provide a mute signal in response to the power-on-reset signal (POR3), wherein the mute signal is the gate control signal.

With respect to claim 4, the combination above discloses the circuit of Claim 3, wherein the timer circuit (SCT) includes a one-shot timer circuit (L1) that generates the reset signal (POR) wherein the one-shot timer circuit is configured to provide the mute signal such that the gate control signal such that the mute signal corresponds to an active logic level when a power supply signal is applied to the circuit, and for a pre-determined period of time thereafter; and such that the mute signal corresponds to an inactive level after the pre- determined period of time.

With respect to claim 5, the combination above discloses the circuit of Claim 1, wherein the sensed signal is the output signal (Vout via 1), and wherein the gate input signal is the trigger signal (from Vout).

With respect to claim 6, the combination above discloses the circuit of Claim 1, wherein the gate circuit is configured to provide the output signal such that a logic level of the output signal (Vout) corresponds to a logic level of the trigger signal (51) if the gate control signal corresponds to an inactive level, and the logical level of the output

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signal (Vout) corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 7, the combination above discloses the circuit of Claim 1, wherein the gate circuit includes an AND gate (9).

With respect to claim 8, the combination above discloses the circuit of Claim 1, wherein the comparator circuit (3) is configured to provide the trigger signal such that the trigger signal corresponds to a first logic level if a voltage associated with the reference signal is greater than a voltage associated with the temperature sensor signal (Vin from 1), and the trigger corresponds to a second logic level if the voltage associated with the reference signal is less than the temperature sensor signal (at 1).

With respect to claim 9, the combination above discloses the circuit of Claim 1, further comprising: a reference circuit (2) that is configured to provide the reference signal in conjunction with the hysteresis-and-output-sensor circuit (5), wherein the hysteresis-and-output-sensor circuit is arranged to modify the reference signal (output of the comparator is viewed as the modified reference signal) if the hysteresis-and-output-sensor circuit is enabled, and wherein the hysteresis-and-output-sensor circuit is disabled if the output signal corresponds to a first logic level.

With respect to claim 10, the combination above discloses the circuit of Claim 9, but fails to disclose the details of the reference circuit. It is well known in the art to use a voltage source coupled to a variable resistor to produce a reference signal. It would have been obvious at the time to use the voltage source of Masumura coupled to a variable resistor for the purpose of adjusting the voltage reference. The resulting

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combination would produce wherein the reference circuit includes: a resistor (variable resistor) that is coupled to the hysteresis-and-output-sensor circuit (via the voltage source) and the comparator circuit (via voltage source); and a current source circuit (variable resistor (voltage through a resistor is a current source) that is configured to provide a current to the resistor.

With respect to claim 11, the first combination above discloses the circuit of Claim 10, wherein the hysteresis-and-output-sensor circuit (5) is configured to provide a hysteresis current to the resistor (in 1) if the output signal corresponds to the second logic level.

With respect to claim 12, the second combination above discloses the circuit of Claim 10, wherein a resistance that is associated with the resistor (variable resistor) is adjustable.

With respect to claim 13, combination above discloses a method for temperature sensing, comprising: employing a circuit to activate hysteresis (5) if a temperature-sensing condition has occurred; and ensuring that the hysteresis is automatically inactive (via La Rosa) when the circuit is powering up.

With respect to claim 14, the combination above discloses the method of Claim 13, further comprising providing a reference signal (2), wherein activating the hysteresis includes modifying the reference signal (via 3), and wherein the hysteresis is active if the output signal corresponds to a first logic level.

With respect to claim 15, the combination above discloses the method of Claim 13, wherein ensuring includes providing an output signal (V_{out}) in response to a gate

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input signal (201) and a gate control signal (at gate), wherein the gate control signal is derived from a power-on-reset signal (POR3), a logic level of the output signal (from 5) corresponds to a logic level of the gate input signal (at 201) if the gate control signal corresponds to an inactive level, and the logical level of the output signal corresponds to a first logic level if the gate control signal corresponds to an active level.

With respect to claim 16, the combination above discloses the method of Claim 15, further comprising: comparing a temperature sensor signal (from 1) to a reference signal (2); and providing a trigger signal in response to the comparison, wherein the gate input signal is based at least in part on the trigger signal (via feedback).

With respect to claim 17, the combination above discloses the method of Claim 15, wherein providing the output signal includes performing a logical AND function (via 9) on the gate input signal (51) and the gate control signal (52).

With respect to claim 18, the combination above discloses the method of Claim 15, further comprising: applying a power supply signal; and providing the gate control signal in response to the power-on-reset signal (POR3), wherein providing the gate control signal (at input to 201) includes: providing the gate control signal such that the gate control signal corresponds to an active logic level when the power supply signal is initially applied, and for a pre-determined period of time thereafter; and providing the gate control signal such that the gate control signal corresponds to an inactive level after the pre-determined period of time.

With respect to claim 19, the second combination above discloses the method of

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Claim 15, further comprising: providing a first current (voltage through resistor); and converting a reference current into the reference signal (via variable resistor), wherein activating the hysteresis includes: providing a hysteresis current if the output signal corresponds to a first logic level; providing substantially no current if the output signal corresponds to a second logic level; and providing the reference current by combining the first current and the hysteresis current.

With respect to claim 20, combination above discloses a circuit for temperature sensing, comprising: means for activating hysteresis (5) if a temperature-sensing condition has occurred; and means for ensuring that the hysteresis is automatically inactive when the means for activating hysteresis is powering up (La Rosa).

With respect to claim 21, the combination above discloses the circuit of claim 22, wherein the circuit for temperature sensing is arranged such that the comparator circuit (3) trips when the temperature sensed by the temperature sensor signal (V_{in} at 1) reaches a predetermined level, and wherein the predetermined level is modified by a predetermined amount when hysteresis is enabled.

With respect to claim 22, the combination above discloses a circuit for temperature sensing, comprising: a comparator circuit (3) that is arranged to provide a trigger signal by comparing a reference signal to a temperature sensor signal; a gate circuit (201) that is arranged to provide an output signal by gating a gate input signal subject to control by a gate control signal, wherein the gate input signal is based at least in part on the trigger signal, and wherein the gate control signal is based at least in part on a power-on-reset signal (POR3); a hysteresis-and-output sensor circuit (5) that is

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configured to control the reference signal in response to a sensed signal, wherein the sensed signal is based at least in part on the output signal; and a temperature sensor signal generation circuit, wherein the temperature sensor signal generation circuit is arranged to provide the temperature sensor signal such that the temperature sensor signal is indicative of a temperature.

With respect to claim 23, the combination above discloses the circuit of claim 22, wherein the temperature sensor signal (V_{in}) is proportional to a temperature.

With respect to claim 24, the combination above discloses wherein the comparator circuit (3) compares the temperature sensor signal (V_{in}) to the reference signal (2) in order to perform a temperature comparison.

With respect to claim 25 the combination above discloses the circuit of claim 24 wherein the hysteresis and output sensor circuit (5) is arranged to provide hysteresis in a range but fails to disclose a range of about 2°C to about 10°C of hysteresis for the temperature comparison when the hysteresis is enabled. It would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange the hysteresis and output sensor circuit to provide hysteresis in the 2°C to about 10°C of hysteresis for the temperature comparison when the hysteresis is enabled, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves routine skill in the art. (See *In re Aller*, 105 USPQ 233.)

With respect to claim 26, the combination above fails to disclose activating at least one of a fan or a heater when the output signal is asserted. It is well known that

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temperature sensing is used in activating fans in HVAC systems. Because the circuit is capable of performing the steps claimed when used in the temperature sensing circuit, it would be obvious to one skilled in the art to use the combination above in a HVAC system for the purpose of controlling the fan or heater using the temperature sensor.

With respect to claim 27, the combination above discloses the circuit of claim 13, wherein ensuring that the hysteresis is automatically inactive when the circuit is powering up is accomplished by disabling the hysteresis until the power up is complete (via La Rosa).

With respect to claims 28-30, this is deemed intended use, because no structural difference would be apparent.

With respect to claim 31, the combination above discloses the method of claim 16, wherein the temperature sensor signal is indicative of a temperature.

With respect to claim 32, the combination above discloses the method of claim 16, wherein the temperature sensor signal is proportional to temperature.

Response to Arguments

4. Applicant's arguments filed 9/28/2010 have been fully considered but they are not persuasive.

With respect to applicant's argument that neither Matsumura nor La Rosa, singly or in combination, discloses, teaches, or suggests, "the hysteresis-and-output sensor circuit is arranged to disable a hysteresis at power up", as recited in Applicant's Claim 1, the Examiner disagrees. The claim merely states the arrangement not function. The

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device according to the claim language merely need have the structure capable of disabling hysteresis at power up. The combination is clearly capable of doing so.

Since the circuit is capable of adjusting a hysteresis voltage, it is respectfully submitted that the circuit of Matsumura is arranged so as to make it capable disabling a hysteresis at power up.

With respect to applicant's argument that the circuit of La Rosa fails to cure the deficiency of Matsumura, the Examiner disagrees. The circuit of La Rosa is a programmable POR circuit with two switching thresholds. Since the adjusting circuit of Matsumura would be able to adjust the La Rosa input to disable it at power-up it deemed to read on the arrangement as claimed. Furthermore, it is clear that 200 of Matsumura disables hysteresis since it is pulled to ground during power-up. Note: the time period of power-up is not clearly defined in the specification or the claim language.

With respect to applicant's argument that, "there is simply no apparent reason, disclosure, teaching, or suggestion that reset signal 52 of FIG. 4 of Matsumura be substituted with a POR signal, from La Rosa or any POR signal at all" the Examiner disagrees. Incorporating a POR circuit that can switch between the one POR and another tailor's the supply voltage to optimum use. Thus "It would have obvious at the time the invention was made to a person of ordinary skill in the art to use the POR reset circuit of Rosa in the voltage detecting circuit for the purpose of incorporating a POR circuit into an integrated circuit that can receive different supply voltage.", since the adjustment circuit of Matsumura is dependent on being controlled by a POR input. The combination would use the POR circuit of La Rosa for the standard functionality of

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a POR circuit, and would be used in place of the reset signal 52 of Matsumura. Reset signal 52 of Matsumura is a reset signal. A POR reset signal is still interpreted as a reset signal that can be replace a standard reset signal at power up. The only difference between a reset signal and a power on reset signal is that a power on reset signal is operative at the power up of the device. A reset signal can come from any device and it is not hindsight to use a reset signal from a POR device that can be switched between to signals to give the optimum performance which is based on the functioning of the voltage in the Matsumura device.

With respect to the declaration under 37 CFR 1.132 the term POR signal has a specific meaning,the Examiner agrees. The arrangement of the POR signal is less precise and does not evoke the totality of POR signal merely only evokes that the structure needs to be capable of implementing the POR signal. The Examiner contends that the combination of La Rosa and Matsumura is sufficient to meet the bounds of the claim limitation.

With respect to applicant's argument that Claim 11 is respectfully submitted to be allowable at least because the proposed combination fails to meet the recitation, "the hysteresis-and-output-sensor circuit is configured to provide a hysteresis current to the resistor if the output signal corresponds to the second logic level", as recited in Claim 11, in conjunction with the recitation, "the reference circuit includes: a resistor that is coupled to the hysteresis-and-output-sensor circuit and the comparator circuit; and a current source circuit that is configured to provide a current to the resistor", as recited in Claim 10, from which Claim 11 depends.", the Examiner disagrees. First the device is

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merely configured, meaning that the components relative to one another are capable of performing the action, not that the action is actually performed. Claim 10 recites that the resistor is in the reference circuit, and the resistor in component (1) of FIG. 1 of Matsumura, is not in reference voltage circuit 2 of Matsumura, but the details of the reference voltage is not disclosed in Matsumura. As stated, it is well known in the art to use a voltage source coupled to a variable resistor to produce a reference signal. It would have been obvious at the time to use the voltage source of Matsumura coupled to a variable resistor for the purpose of adjusting the voltage reference. Thus the resulting combination would produce the claim of claim 10.

With respect to claim 25, the Examiner contends that the workable range is obvious expedient.

With respect to claim, "employing a circuit to activate hysteresis if a temperature-sensing condition has occurred". The Examiner points out the temperature sensor of the claimed invention is shown with not structure but only as an input and thus not given patentable weight since it is interpreted only as a voltage value.

With respect to claims 14-19 and 26-34, these are rejected for similar reasons.

With respect to claim 20, this claim is rejected for reasons similar to those stated above with regard to Claim 13.

With respect to claim 32, this is rejected for similar reasons as above pertaining to the temperature sensor not having patentable weight because it is discloses only as an input signal.

With respect to claim 26, the claim is deemed intended use because: First it is well known that Fan and heating systems require temperature sensing. See applicant's background. It is well known to use a temperature sensor circuit in a HVAC circuit. Using the apparatus in a temperature producing circuit would inherently accomplish the method steps in claim 26 and is deemed obvious expedient to one skilled in the art, to use a similar circuit in a HVAC system. Thus using the apparatus in an HVAC unit would produce the claimed steps discloses as the method of the invention.

With respect to applicant's arguments, concerning the structure that definitely performs the function under the recited circumstances, the Examiner points out that the device is capable of performing the disable at power-up. The device does not need to be completely redesigned to function accordingly but can function accordingly under the condition the signal is powered up. i.e. where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235. In this situation the disablement of hysteresis is the object of the workable range, whereby the disablement at power-up is the routine experimentation.

With respect applicant's argument that in order to disable hysteresis at power up, the combination would have to be redesigned in such a way that it detected that power up was occurring, have this detection provided to circuitry that controls the hysteresis, and have circuitry capable of turning on and off hysteresis based on the detection that power up is occurring, The Examiner points out that power on is detected via the reset input at 52 detecting the POR signal produced via POR1, POR2 and POR3 of La rosa,

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this signal is provided to circuitry (6) that controls hysteresis (in figure 1 labeled hysteresis control circuitry), and is capable of turning on and off hysteresis based on the detection that power up is occurring via the hysteresis control circuitry. The combination does have such a structure. The proposed structure would not change the principle of operation of Matsumura.

With respect to applicant's argument that there is no apparent reason or suggestion that hysteresis would be based on power up in any way, the Examiner disagrees. The hysteresis is based on a reset signal. A POR signal is a type of reset signal. The adjustment of hysteresis in the present combination and in Matsumura is simply a matter of when switch 200 is open or closed. Since the switch being open or closed is based on the power up signal the hysteresis is based on the Power up signal. Wherein the applicant argues the a reset signal not interchangeable with a power on reset signal the Examiner argues that a power on reset signal is merely a type of reset signal (i.e. a subset of a reset signal) and thus can replace the reset signal.

With respect to applicant's argument that the circuit of Matsumura is pulled to ground prior to power up, and is not pulled to ground during power up, the Examiner explains the that the power up period can be interpreted to mean the point from which Matsumura is pulled to ground up until the point of full power up since the period of time is not clearly defined in the specification. (ie. the catalyst for power up is part of the power up cycle.) With regard to the declaration of Perry Lorenz, the catalyst is not an arbitrary time but the start of a period of time of power up. Likewise, the POR signal, can be interpreted as the start of Power on.

With respect to applicants argument that the proposed modification would render the invention incapable of performing its proposed function, the Examiner disagrees. The reset is not specifically mentioned in Matsumura as occurring at any specific time on listed as a reset signal. The POR of La Rosa limits the reset signal to a POR signal and as such (since a POR is a subset of a reset signal) would not render the invention incapable of controlling hysteresis. The reset signal of Matsumura 52 is limited to being at a specific time.

With respect to claim 11, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

With respect to claim 25, the workable range of 2 to 10 degrees Celsius is merely obvious expedient through routine experimentation. The temperature sensor signal is merely a input voltage, and does not change the circuitry. Since the temperature sensor is not claimed, then the limitation is some voltage that is input into the system limited to a range of temperatures. The range of temperatures which the circuit accomplished hysteresis is obvious.

With respect to claim 13, argument is persuasive, however any circuit meets the limitation because the condition is prefaced on if a temperature sensing condition has occurred. If a temperature sensing condition has not occurred hysteresis can or can not be activated.

With respect to claim 26, the rejection above addresses the intended use argument.

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Furthermore, since the claim 1, and 24 is a structure claim and not a method claim, the circuit merely needs to be capable of performing the function. Since a temperature comparison is manifested through a comparison of voltages, the present structure is capable of achieving the claim limitations.

Allowable Subject Matter

5. Claims 33 and 34 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 33 and 34, the prior art of record fails to suggest or disclose the method of claim 13, wherein the temperature-sensing condition is a temperature comparison in which a determination is made as to whether a temperature has reached a predetermined condition wherein the predetermined level is modified by a predetermined amount when hysteresis is enabled.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAREEM E. ALMO whose telephone number is (571)272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khareem E Almo/
Examiner, Art Unit 2816
/Lincoln Donovan/

Supervisory Patent Examiner, Art Unit 2816